An Energy-Efficient and High Gain Low Noise Amplifier for Receiver Front-Ends

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Abstract— This paper introduces a high gain CMOS Low Noise Amplifier (LNA) for RF front-end receiver and present simulation performance in the TSMC 0.18um CMOS technology. In the LNA design, we employ an energy efficient metric in order to realize low power as well as high gain. In addition, we employ a combination of the Partial Source Degeneration (PSD) technique, reuse current and boosting inductor to enhance the performance and gain. Our simulation results at 1.9 GHz demonstrate a forward gain of 26.23 dB with a Noise Figure (NF) of 1.038 dB while drawing 7.8 mW from a 1.2V source supply. The simulations also validate a high linearity Input Third-Order Intercept Point (IIP3) of 6.87m dBm, with input-referred 1dB compression -8.99 dBm.

Key Words— CMOS; TSMC 0.18um CMOS; Partial Source Degeneration PSD; boosting Inductors; Gain, Linearity.

I. INTRODUCTION

The fast growing rate of reproduction of mobile computing devices has supplied the demand for wireless local area networks (WLANs). The front-end receiver is becoming more and more important in a wireless communication system. As the expanded application, customers demand requires WLAN devices that are cheap, small size and light weight, as well as long battery life. It intends that customers want low-cost, low-voltage and small-scaled personal wireless communication equipment. The CMOS technology is being utilized to fulfill these requirements in order to integrate the RF front-end functions on a single die. Therefore RF-CMOS integrated circuit turns to be the hot spot area at present because of the characteristics of low-cost, low power and ease-integrated. There are a lot of topologies and design techniques of RF circuits have a great achievement has been acquired [1, 2, 7, 8].

RF receiver is at the front-end of wireless communication system. There are three types of wireless receivers: super heterodyne receivers, zero-intermediate frequency receivers, low-intermediate frequency receivers. The first active device to amplify the signal in the RF front-end is the LNA that has the significant impact on noise performance in the whole receiver since the first stage in the Cascaded system has dominated input-referred noise so LNA has major impact in the front-end receiver as well [1, 2, 3]. So, the low noise amplifier is considered as an essential RF front-end building block, which is considered a key stone factor in determining the noise figure of the system. Fig.1 shows a block diagram of an RF front-end receiver. The first active device to amplify the signal in the RF front-end is the LNA [2, 3].

The most important parameter in the LNA design it is the noise and the most important noise in the RF integrated circuit is the thermal noise – when operating at high frequencies, the thermal noise is more influential than the flicker noise. As we know, most of the thermal noise comes up from the resistance. In communication systems have mainly two parameters that describe their performance: power and the bandwidth. In this paper we have to trade-off among these two parameters. The main challenge in the front-end receiver lies in maintaining high gain, noise figure, and linearity at minimum power consumption with lower supply voltage. This paper presents the design and implementation of an LNA for 1.9-GHz LNA applications simulated in an in TSMC 0.18um CMOS. This LNA has lower power consumption by using current reused topology and energy efficient metric which used in [7].
This metric shows us the critical width which can be used to get a higher gain with lower power consumption. Moreover, in order to share the operating current and reduce current consumption, two-stage common source amplifier has been used in the current reuse topology. In this paper, in order to enhance the performance and gain at 1.9GHz we use the new Partial Source Degeneration (PSD) technique and a current reused topology of a two-stage common source amplifier to share the operating current. The organization of this paper is described as follows. In section 2, energy efficient metric for RF tuned circuit. Section 3, the schematic and characteristic of the proposed LNA are presented. Simulation results for proposed LNA are proposed in section 4. The conclusion is summarized in section 5.

II. ENERGY EFFICIENT METRIC FOR RF TUNED AMPLIFIER.

We use the same metric in [7] to quantify the energy efficiency of gain in our design. In this paper, we use this metric to identify the width of transistor which has the lowest power consumption and higher gain. It gives us indication about the size of a transistor and an appropriate biased voltage. A fundamental tenet of the metric is that only the total gain and power consumption affect energy efficiency. So the general energy-efficiency metric:

\[
Efficiency = \frac{\log(gain)}{Power}
\]

Fig. 2 shows the tuned LC amplifier circuit that consists of tank LC which has a resonance frequency at the 1.9G Hz.

Fig. 3 shows the Gain of the tuned amplifier versus the width of transistor and the power consumption. Fig. 4 presents the corresponding energy efficiency using the metric (1). We see that at the 1.9 GHz in the TSMC 0.18um CMOS process, the maximum energy efficiency of a tuned amplifier occurred at certain size to get us a maximum gain with lower power consumption. This conclusion motivates us to use the appropriate width and bias voltage in order to get the highest performance of the LNA.

III. LOW NOISE AMPLIFIER (LNA) DESIGN

In the LNA circuit, there are many factors that need to be considered in the LNA design. Perhaps the most important ones are gain and the noise factor. The most important challenge in the LNA design is the linearity issue, which influences the performance and the stability of our design which should be stable and realistic. Actually, we cannot separate these parameters from each other, since they have related issues with other parameters in communication like the relationship between the power supply and the gain of LNA or non-linearity.

We start our design to set the length of the transistor to the minimum of the technology and using the metric in the previous section to find the best width. As shown in fig 4; we choose a value for width as fellow:

\[ W_{opt} = 110 \text{ uW} \]

Once we got the total width, the inductors chosen to better fit the impedance matching. We can present the partial source degeneration technique [4] by using two parallel transistors in Common Source configuration as shown in fig. 5.

Fig.6 shows the proposed LNA design using a current reuse to achieve minimum power consumption, partial source degenerate and Boosting inductors topologies. \( M_{N1} \) and \( M_{N2} \) transistors are both common source configurations. \( M_{N1} \) and \( M_{N2} \) Cascade common source amplifiers use the same supply
current to reduce dc current consumption and both are cascoded with $M_{N3}$ transistor using the current reuse to save the dc current also. $C1$ capacitor works as a dc block. The cascoded $M_{N1}$ and $M_{N2}$ transistors give us high gain and improve input output reverse isolation with cascoded $M_{N3}$ transistor. We use $L_M$ “Mutual Coupled Degenerated resonant tank, thus increasing the choke isolation. Furthermore we used boosting transistor to improve the input match with partial degenerate source, improve the linearity and increase high reverse isolation [4, 8]. The transistors $M_{P1}, M_{N5}$ and $M_{N4}$ form a CMOS voltage divider to provide bias voltage to the gate of the amplifier, a choke inductor in parallel with a tank capacitor to form a resonant tank, thus increasing the choke isolation.

The new input impedance can be obtained from the equivalent impedance of the circuit in Fig.6. Then, the equivalent input impedance assumes the form:

$$Z_{eq} = \frac{Z_{cgs1}Z_{cgs2}}{Z_{cgs1} + Z_{cgs2}} + Z_{ls} + g_{m2}Z_{cgs2}Z_{ls}$$

So, we could observe from the above equation at resonant frequency:

$$Z_{eq} = \frac{1}{\omega_{cgs1}(\omega_{cgs1} + \omega_{cgs2})} - \frac{r_s}{\omega_{cgs1}(\omega_{cgs1} + \omega_{cgs2})}$$

$R_{in}$ is a real partition controlled by the degenerated transistor. So, $Z_{eq}$ becomes dependent of $g_{m2}$.

$$R_{in} = \frac{g_{m2}(\omega_{cgs1} + \omega_{cgs2})}{C_{gs2}}$$

Then, extra capabilities to clarify adjust the circuit input impedance, besides the increasing in the gain. As we know, the tradeoff between NF and gain of the amplifier. Increase in the gain means decrease in the Noise Factor [2, 3], so improvement in gain gives us improve in noise figure. Furthermore, due to

$$\omega_r = \frac{g_{m2}}{C_{gs2}} \propto \frac{1}{L^2} (V_{gs2} - V_{th2})$$

There is compromise to increase IIP3 due to

$$\text{IIP3} \propto (V_{gs2} - V_{th2}) \implies I_D \propto \frac{W}{L} (V_{gs2} - V_{th2})^2$$

Fig 5. Proposed LNA input impedance electrical model

Fig 6. Proposed New Partial Source Degenerate Schematic

IV. EXPERIMENTAL RESULTS

In this section, we present the simulation results of LNA circuit. The presented LNA circuit is designed by 0.18 $\mu$m TSMC CMOS RF process and is simulated by a Cadence tool. The proposed LNA design described in Section 3 is operated around 1.9 GHz. The circuit is biased at 1.2V supply voltage. All simulation results were made with 50 ohms input port and 50 ohms at the output port. S-Parameters simulation is used to measure the small signal gain. As clearly seen in Fig. 7, the circuit has a gain of 26.23 dB at a 1.9 GHz frequency.

It is also shown that it consumes 6mA from a 1.2V supply

![Fig.7. Forward Gain S21](image-url)
source. For any LNA design it is ideal to have our NF as low as possible. We used the S-Parameter to find the NF as shown in the Fig.8. As clearly seen from the Fig.8 the circuit has NF of 1.038 dB at 1.9G Hz. The 1-dB compression point is a good measure for the LNA linearity. The Spectre RF simulator was used for the 1-dB compression and IIP3 point simulation.

As seen in the Fig. 9, an IIP3 of 6.875m dBm at 1.9G Hz is obtained. The plot shown in Fig. 9 was created using two tones technique. As seen in the Fig. 10, a1-dB compression of -8.998 dBm at 1.9G Hz is obtained. These results outperform results reported in [4, 5, 6].

V. CONCLUSION

The primary goal of any LNA is to obtain a high gain with a very low noise. So, in this paper we report the work that tries to get the high gain and low noise figure of a 1.9G Hz CMOS LNA.

We achieved a high gain 26.23 dB and 1.03 dB low noise factor with improving the linearity IIP3. Furthermore, the LNA demonstrates a high stability and a very low Noise figure which shows that it is suitable with a competitive Linearity, a low noise figure, reasonable gain, and stability are combined by the LNA without oscillation over entire useful frequency range.

ACKNOWLEDGMENT

I would like to express my sincere gratitude to my Prof. Fathi Salem, Department of Electrical and Computer Engineering, Michigan State University, USA, under whose supervision this research was undertaken.

REFERENCES

Zaid Albataineh received the B.S. degree in electrical engineering from the Yarmouk University, Irbid, Jordan, in 2006, and received the M.S. degree in the communication and electronic engineering from the Jordan University of Science and Technology JUST, Irbid, Jordan, in 2009. He is currently pursuing the Ph.D. degree in electrical and computer engineering department, Michigan State University (MSU), USA. His research interests include Blind Source Separation, Independent Component analysis, Nonnegative matrix Factorization, Wireless Communication, DSP Implementation, VLSI, Analog Integrated Circuit and RF Integrated Circuit.

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Dr. Salem has served in many capacities over the years. He was an Associate Editor and Guest Editor for numerous IEEE and other transactions including the IEEE Circuits And Systems, IEEE Neural Networks, the Journal of Circuits, Systems, and Computers, and the Journal of Computer and Electrical Engineering. He was the Chairman of the Engineering Foundation Conference on Qualitative Methods for Nonlinear Dynamics. He served in several capacities in several conferences including the General Chair of the IEEE Midwest Symposium on Circuits and Systems in Lansing, Michigan in 2000.

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Dr. Salem has published more than 200 technical papers. He was the Co-Editor of the Book, Dynamical Systems Approaches to Nonlinear Problems in Circuits and Systems, (SIAM, 1988). He was the Guest Co-Editor of the IEEE-CAS Special Issue on Bifurcations and Chaos in Circuits and Systems July 1988 (with T. Matsumoto), the Special Issue on Micro-Electronic Hardware Implementation of Soft Computing: Neural and Fuzzy networks with Learning, in the Journal of Computers and Electrical Engineering, July 1999 (with T. Yamakawa), and the Special Issue on Digital and Analog Arrays, in the Journal of Circuits, Systems, and Computers, August 1999 (with M. Ahmadi). He is a co-inventor of over 10 patents on adaptive nonlinear signal processing, neural architectures, learning, and low-power CMOS VLSI implementations. His current research interests include: Adaptive sensing and actuation electronic ICs; RF-electronic circuits and systems; and Blind Equalization, Separation, and Recovery processing.; Dr. Salem became a Fellow of the IEEE in 1996. He is a recipient of the IEEE CAS Golden Jubilee Award (1999), the IEEE Third Millennium award (2000), The CAS Darlington Best Paper Award (2001). With a Team of students, he also received the U.S. Semiconductor Research Corporation (SRC) Phase II Finalist award (2000). Dr Salem served as a Distinguished Lecturer of the IEEE CAS society for 2000-2001.